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"DC-CONDEX - Execução Condicional de Instruções com Compactação Dinâmica de Código"

VLIW architectures provide a way to explore the instruction level parallelism. But mapping a VLIW instruction set architecture to implementations with different hardware latencies and varying levels of parallelism is not generally possible. This problem is known as *object code compatibility*. The DIF concept is a way to overcome this, as it allows code compaction on run time, so that if it is necessary to re-execute some block, it can be done in VLIW mode. The Dynamically Trace Scheduled VLIW architecture uses the DIF concept. The instructions from the program in execution are scheduled to a structure called *Scheduling List*, and are further flushed to a VLIW Cache. The Conditional Execution concept, used by the CONDEX-1 architecture allows a code compaction with the possibility of instructions from different basic blocks to share long instructions. In this kind of machine, the instructions compacted are associated to condition registers that, in run time, can define which of them are really executed each cycle. This work sugests na architecture with conditional execution, the DC-CONDEX (CONditional EXecution with Dynamic Compaction) that compacts code in run time, using some features of the DTSVLIW architecture. To analyse the performance of DC-CONDEX, we developed a simulator of the architecture and used five programs of the benchmark SPEC95.